IN THE CLAIMS

1. (Currently amended) A non-volatile memory device comprising:

a memory gate pattern and a selection gate pattern separated from each other and arranged on a semiconductor substrate,

the memory gate pattern comprising;

a tunnel dielectric layer, a floating gate, a first inter-gate dielectric, and a control gate electrode, which are sequentially stacked; and

the selection gate pattern comprising;

a gate dielectric layer, a bottom gate pattern, a second inter-gate dielectric, and a top gate pattern, which are sequentially stacked, wherein ~~the~~ a width of the second inter-gate dielectric is narrower than that of the bottom gate pattern, and wherein the second inter-gate dielectric extends from one sidewall of the selection gate pattern to approximately center thereof.

2. (Cancelled)

3. (Previously presented) The non-volatile memory device of claim 1, wherein the control gate electrode and the top gate pattern further include a mask conductive layer, and wherein the mask conductive layer is formed on the first and second inter-gate dielectrics.

4. (Original) The non-volatile memory device of claim 1, wherein the top gate pattern is electrically connected to the bottom gate pattern.

5. (Currently amended) A non-volatile memory device comprising:

a device isolation layer disposed on a semiconductor substrate to define a plurality of active regions;

selection lines extending across the active regions, the selection lines each including a bottom gate pattern, a second inter-gate dielectric and a top gate pattern, which are sequentially stacked; and

a plurality of word lines disposed between the selection lines to extend across the active regions and including a floating gate pattern, a first inter-gate dielectric and a control gate electrode, which are sequentially stacked,

wherein ~~the~~ a width of the second inter-gate dielectric is narrower than that of each selection line, and wherein the second inter-gate dielectric extends from one sidewall of the selection line to approximately center of the selection line.

6. (Cancelled)

7. (Original) The non-volatile memory device of claim 5, wherein the floating gate pattern is interposed between each of the active regions and the word line, and wherein the bottom gate pattern is disposed under the top gate pattern to extend across the active regions.

8. (Original) The non-volatile memory device of claim 5, wherein the second inter-gate dielectric crosses over the active regions.

9. (Original) The non-volatile memory device of claim 5, further comprising:

a mask conductive layer disposed between the second inter-gate dielectric and the top gate pattern; and between the first inter-gate dielectric and the control gate electrode.

10. (Original) The non-volatile memory device of claim 5, wherein the first and second inter-gate dielectrics include at least a single dielectric layer having a dielectric constant higher than that of a silicon oxide layer.

11. (Original) The non-volatile memory device of claim 5, further comprising:

a second active region defined by the device isolation layer; and

a peripheral gate pattern crossing over the second active region,

wherein the peripheral gate pattern includes a bottom conductive pattern and a top conductive pattern sequentially stacked to be electrically connected to each other.

12-19. (Cancelled)

20. (Currently amended) A non-volatile memory device comprising:

a semiconductor substrate;

a gate line having two sidewalls formed on the substrate, the gate line including:

a gate dielectric layer, a bottom gate pattern, an inter-gate dielectric and a top gate pattern, which are sequentially stacked on the substrate,

wherein ~~the~~ a width of the inter-gate dielectric is narrower than that ~~the~~ of the bottom gate pattern, and wherein the inter-gate dielectric extends from only one sidewall of the gate line towards the other sidewall.